CLAIMS

What is claimed is:

1. A driver set for a cross point memory array comprising:

a semiconductor substrate with an active surface in the x-direction and y-direction directions;

a plurality of line driver groups formed on the active surface of the substrate and stacked in the y-direction, each line driver group having transistors in various positions;

a plurality of y-direction lines on a first fabrication layer above the active surface of the semiconductor substrate, each y-direction line electrically connecting the transistors of a line driver group to transistors of other line driver groups that share the same relative position;

a plurality of first x-direction lines on a second fabrication layer above the active surface of the semiconductor substrate that electrically connects the transistors of a line driver group to each other;

a plurality of second x-direction lines on the second fabrication layer, each second x-direction line electrically connecting the line drivers in each line driver group;

a plurality of third x-direction lines on the second fabrication layer, each third x-direction line electrically connected to a single line driver.

2. The driver set of claim 1, wherein:

the first fabrication layer is below the second fabrication layer.

3. The driver set of claim 1, wherein:

each of the third x-direction lines are in electrical contact with a row of memory cells.

4. The driver set of claim 1, wherein:

the plurality of y-direction lines are electrically connected to a secondary decoder that selects a line driver in each line driver group.

5. The driver set of claim 1, wherein:

the plurality of second x-direction lines are electrically connected to a primary decoder that selects one line driver group out of the plurality of line driver groups.

6. The driver set of claim 1, wherein:

at least some of the electrical connections between the transistors of a line driver group to transistors of other line driver groups that share the same relative position are made by electrically connecting the transistor's gates.

7. The driver set of claim 6, wherein:

at least some transistors within a line driver group share a common node; and

some of the electrical connections between the transistors of the line driver groups are made by electrically connecting the common node of some transistors.

8. The driver set of claim 7, wherein:

some of the electrical connections between the line drivers in each line driver group are made by connecting the common node of some transistors in the line driver group.

9. The driver set of claim 6, further comprising:

a plurality of fourth x-direction lines on the first fabrication layer, each fourth x-direction line in a line driver group electrically connected to the second x-direction

line in a driver group such that the second x-direction line can electrically connect the line drivers in each line driver group.

10. A driver set for a cross point memory array comprising:

a plurality of line driver groups that are electrically connected to

a reference voltage;

a primary decoder;

a secondary decoder; and

a memory array;

wherein the electrical connections are achieved in two metallization layers.

11. The driver set of claim 10, wherein:

the plurality of line driver groups drive contiguous conductive array lines.

12. A driver set comprising:

a plurality of line driver groups that are stacked in a first direction, each line driver group having a plurality of line driver stages, each line driver stage having two line drivers such that the first line driver has transistors that share a common node

with transistors of the second line driver, wherein each transistor in each line driver group has a relative position;

a first metal layer that

electrically connects all the transistors in the same relative position to each other with conductive lines in the first direction, and

provides an extension for one line driver stage in a second direction, the second direction being orthogonal to the first direction; and

a second metal layer that

electrically connects all the transistors to a memory array, and

electrically connects all the line driver stages in each line driver group, whereby the electrical connection in the one line driver stage is made via the extension.

13. A re-writable cross point memory array comprising:

a semiconductor substrate with an active surface in the x and y directions;

a plurality of line driver groups formed on the active surface of the substrate and stacked in the x and y directions, each line driver group having transistors in various positions and no more than two metallization layers;

one or two x-direction conductive layers that include conductive array lines, the conductive array lines electrically connected to the x direction line driver groups; and

one y-direction conductive layer that include conductive array lines, the conductive array lines electrically connected to the y direction line driver groups; and

memory plugs.

14. The re-writable cross point memory array of claim 13, wherein:

the line driver groups are underneath the conductive layers.

15. A re-writable cross point memory array comprising:

a semiconductor substrate with an active surface in the x and y directions;

a plurality of line driver groups formed on the active surface of the substrate and stacked in the x and y directions, each line driver group having transistors in various positions, and no more than three metallization layers;

three x-direction conductive layers that include conductive array lines;

two y-direction conductive layer that include conductive array lines; and

memory plugs.

16. The re-writable cross point memory array of claim 14, wherein:

the line driver groups are underneath the conductive layers.

17. A cross point memory array comprising:

at least one x-direction conductive layers that include conductive array lines that terminate at line ends;

at least one y-direction conductive layer that include conductive array lines;

memory plugs; and

a plurality of x-direction line drivers that drive x-direction conductive array lines;

wherein at least some x-direction line drivers connect with the x-direction conductive lines at a location other than the line ends.

18. The cross point memory array of claim 17, wherein:

the locations of the connections between the x-direction line drivers and the x-direction conductive lines are substantially in the middle of the x-direction conductive lines.

19. A cross point memory array comprising:

memory plugs having tops and bottoms;

a plurality of y-direction conductive array lines in electrical contact with the tops of the memory plugs;

a plurality of x-direction conductive array lines in electrical contact with the bottoms of the memory plugs;

wherein the plurality of x-direction conductive array lines includes an array cut that is where two contiguous x-direction conductive array lines are spaced further apart than other contiguous x-direction conductive array lines.

20. The cross point memory array of claim 19, further comprising:

a plurality of x-direction line drivers underneath the conductive array lines, each x-direction line driver in electrical contact with an x-direction conductive array line; and

a plurality of y-direction line drivers underneath the conductive array lines, each y-direction line driver in electrical contact with a y-direction conductive array line;

wherein the array cut provides enough space to connect the plurality of y-direction conductive array lines to the plurality of y-direction line drivers through the array cut.

21. The cross point memory array of claim 19, wherein:

the array cut is substantially in the middle of the plurality of x-direction conductive array lines.

22. The cross point memory array of claim 20 wherein:

the x-direction conductive array lines terminates at line ends;

the x-direction line drivers connect with the x-direction conductive array lines away from the line ends.

23. The cross point memory array of claim 22, wherein:

the x-direction line drivers connect with the x-direction conductive lines substantially in the middle of the line ends.

24. The cross point memory array of claim 23, wherein:

the array cut is substantially in the middle of the plurality of x-direction conductive array lines.

25. The cross point memory array of claim 20, further comprising:

exactly two metallization layers underneath the conductive array lines.

26. The cross point array of claim 25, further comprising:

a second group of memory plugs having tops and bottoms, the bottoms being in electrical contact with the plurality of x-direction conductive array lines;

a second plurality of x-direction conductive array lines in electrical contact with the tops of the second group of memory plugs;

a third group of memory plugs having tops and bottoms, the bottoms being in electrical contact with the second plurality of x-direction conductive array lines;

a second plurality of y-direction conductive array lines in electrical contact with the tops of the third group of memory plugs;

a fourth group of memory plugs having tops and bottoms, the bottoms being in electrical contact with the second plurality of y-direction conductive array lines; and

a third plurality of x-direction conductive array lines in electrical contact with the tops of the fourth group of memory plugs.